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Filed: December 4, 2001

VERIFICATION OF A TRANSLATION

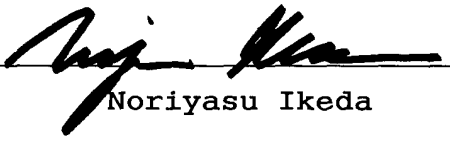
I, the below named translator, hereby declare that:

My name and post office address are as stated below;

That I am knowledgeable in the Japanese language in which the below identified Japanese application was filed, and that I believe the English translation of the Japanese application No. 368539/2000 is a true and complete translation of the above identified Japanese application as filed.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: July 16, 2003

Full name of the translator: 
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JAPAN PATENT OFFICE

This is to certify that the annexed is a true copy of the following application as filed with this Office.

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Mitsubishi Denki Kabushiki Kaisha

October 3, 2001

Commissioner,
Japan Patent Office

Kozo Oikawa

Certificate No. P 2001-3090375

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[Other Matter] Patent application related to the result of government-commissioned research (commissioned research related to "Research and Development of Ultra High Density Electronic SI Technology - Development of Energy Use Rationalization Technology" by New Energy and Industrial

Technology Development Organization, 1999, subject to Industrial Revitalization Law, Article 30)

[Official Fee]

[Deposit Number] 012416

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[List of Presented Documents]

[Name] Specification 1

[Name] Drawing 1

[Name] Abstract 1

[Registration Number of General Power of Attorney] 9001569

[Proof] Required

(Translation)

[Name of Document] SPECIFICATION

[Title of Invention] SEMICONDUCTOR CHIP LAMINATING/MOUNTING METHOD

[Claim for Patent]

[Claim 1] A semiconductor chip laminating/mounting method for sequentially laminating and mounting a plurality of semiconductor chips each having an electrode surface, comprising the steps of:

activating the electrode surfaces of the semiconductor chips opposite to each other;

positioning the semiconductor chips opposite to each other;

laminating and bonding the semiconductor chips opposite to each other by pressing without forming a reaction layer; and

collectively heating the semiconductor chips so as to form the reaction layer after lamination and bonding of all the semiconductor chips are completed.

[Claim 2] A semiconductor chip laminating/mounting method for sequentially laminating and mounting a plurality of semiconductor chips each having an electrode surface, comprising the steps of:

activating the electrode surfaces of the semiconductor chips opposite to each other;

positioning the semiconductor chips opposite to each other;

laminating and bonding the semiconductor chips opposite to each other by pressing and applying supersonic wave without forming a reaction layer; and

collectively heating the semiconductor chips so as to form the reaction layer after lamination and bonding of all the semiconductor chips are completed.

[Claim 3] A semiconductor chip laminating/mounting method as

claimed in claim 1 or 2, wherein the electrode surface includes solder formed on a bump on the semiconductor chip.

[Claim 4] A semiconductor chip laminating/mounting method as claimed in claim 1 or 2, wherein the electrode surface comprises solder containing an active component formed on a bump on the semiconductor chip by electroless plating.

[Claim 5] A semiconductor chip laminating/mounting method as claimed in any one of claims 1 to 4, wherein the reaction layer comprises a bonding layer of solder.

[Claim 6] A semiconductor chip laminating/mounting method as claimed in any one of claims 1 to 5, wherein the reaction layer is uniformly formed between the semiconductor chips opposite to each other.

[Claim 7] A semiconductor chip laminating/mounting method as claimed in any one of claims 1 to 6, wherein the activating step is carried out in order to remove an organic substance on the electrode surface.

[Claim 8] A semiconductor chip laminating/mounting method as claimed in any one of claims 1 to 7, wherein the pressing step is carried out in the manner such that the bonding is performed via interatomic force by making the activated electrode surfaces approach each other at an interatomic distance.

[Claim 9] A semiconductor chip laminating/mounting method as claimed in any one of claims 1 to 8, wherein the activating step is carried out by an atomic beam of an inactive gas excited by plasma.

[Claim 10] A semiconductor chip laminating/mounting method as claimed in any one of claims 1 to 8, wherein the activating step is carried out by irradiating radical fluorine.

[Claim 11] A semiconductor chip laminating/mounting method as claimed in any one of claims 1 to 8, wherein the activating step is carried out by sputtering.

[Claim 12] A semiconductor chip laminating/mounting method as claimed in any one of claims 1 to 8, wherein the activating step is carried out by heat treatment in a reduction gas.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

This invention relates to a semiconductor chip laminating/mounting method and, in particular, to a three-dimensional semiconductor chip laminating/mounting method.

[0002]

[Prior Art]

In a semiconductor laminating/mounting technique of the type described, direct lamination of semiconductor chips is carried out by placing a small-sized semiconductor chip on a circuit surface of a large-sized semiconductor chip via an adhesive, establishing electrical connection by wire bonding, and then sealing.

[0003]

By the above-mentioned lamination, a semiconductor device of a high-density mounting structure is realized. One of important factors is to assemble the semiconductor chips without damaging the circuit surface due to the shock during the bonding.

[0004]

In order to achieve the above-mentioned object, the semiconductor chips to be laminated must sequentially be reduced in size as a prerequisite for lamination. In order to achieve a high-density semiconductor device, the semiconductor chips must be reduced in thickness.

[0005]

Fig. 3 shows an existing semiconductor laminating/mounting technique.

Specifically, the figure shows a sectional view of a semiconductor device in which laminated semiconductor chips are connected to each other by wire-bonding.

[0006]

On an interposer 12, a semiconductor chip 1a and a semiconductor chip 1b smaller in size than the semiconductor chip 1a are laminated by Ag paste 13, electrically connected by the use of wire-bonding wires 11, sealed in mold resin 15, and provided with external terminals (solder bumps 14). Thus, the semiconductor device is formed.

[0007]

However, the semiconductor device produced by the above-mentioned method achieves the electrical connection via the wire bonding. Therefore, only the semiconductor devices different in chip size from each other can be laminated. Moreover, the semiconductor chips can not be superposed in a face-down style.

[0008]

Accordingly, an area for the wire bonding is required so that high-density mounting is not sufficiently achieved.

[0009]

In addition, the wire bonding for electrically connecting the semiconductor chip and the interposer after lamination of the semiconductor chips imposes a large load upon the circuit surface of the semiconductor chip laminated at a lower stage so that the semiconductor chip may be broken.

[0010]

On the other hand, as another existing semiconductor laminating/mounting technique, there is a method for assembling the semiconductor devices adapted to be laminated and thereafter laminating the semiconductor devices without directly laminating the semiconductor chips.

[0011]

Fig. 4 shows the existing semiconductor laminating/mounting technique mentioned above.

[0012]

A semiconductor chip 1 is superposed on an interposer 12, and solder bumps 14 are formed. The semiconductor chip 1 thus superposed and the interposer 12 are processed into a reduced thickness within the range of standoff of the solder bumps 14 so as to allow lamination. A predetermined number of semiconductor devices thus obtained are laminated and superposed. Thereafter, collective reflowing is carried out and electrodes are connected. Herein, the reference numeral 16 represents flux.

[0013]

In the above-mentioned method, however, the interposer must be used for each semiconductor chip to be laminated. Therefore, a thin semiconductor device can not be obtained. Further, although collective reflowing is carried out upon the lamination, self-alignment is possible. Specifically, the lamination is possible only in case where use is made of a relatively large solder bump for a pitch between 1 mm and 0.5 mm sufficient to absorb variation in flatness or positional accuracy.

[0014]

Moreover, as another existing semiconductor mounting technique, there is a method for laminating semiconductor chips having a fine pitch. The existing semiconductor mounting technique is illustrated in Fig. 5.

[0015]

As illustrated in Fig. 5, semiconductor chips 1 each having a circuit surface 6 and a back surface 7 are positioned and bonded with solder 4. Thereafter, another semiconductor chip 1 to be laminated next is positioned and bonded with solder. Because of the fine pitch, the self-alignment effect can not

be expected by collective reflowing upon multi-stage lamination. Consequently, it is inevitable to sequentially carry out solder bonding. Herein, the reference numeral 2 represents a penetration electrode and the reference numeral 3 represent a bump. The reference numeral 5 represents a solder bonding layer.

[0016]

In the above-mentioned method, one of important factors is to improve the positioning accuracy of the electrodes of the semiconductor devices superposed in a multi-layer structure, to sufficiently consider the composition of the electrode material of the semiconductor chip, and to reduce thermal hysteresis during laminating and mounting.

[0017]

However, in the existing laminating method, it is difficult to miniaturize the semiconductor device.

[0018]

Further, in case where the semiconductor chips having very fine electrodes are mounted, bonding by collective reflowing after lamination of a predetermined number of chips is difficult. Consequently, the semiconductor chips must be sequentially laminated and bonded by solder.

[0019]

In this event, the bonding portion in the first lamination is applied with heat at several times of solder bonding until the final lamination. Therefore, the bonding portions at the first stage and the final stage are different in structure and are degraded in reliability due to repeated heating.

[0020]

Taking the above-mentioned circumstances into consideration, it is necessary to take any countermeasure, for example, to change electrode specification of the interposer at every stage of lamination. This inevitably results in high cost.

[0021]

[Problem to be Solved by the Invention]

In view of the above-mentioned disadvantages in the existing techniques, it is an object of this invention to provide a semiconductor chip laminating/mounting method for laminating and mounting semiconductor chips with very fine electrodes, which enables mounting by collective heating reflowing after lamination and which assures production of uniform and highly-reliable bonding portions.

[0022]

In order to achieve the above-mentioned object, this invention provides a semiconductor chip laminating/mounting method for sequentially laminating and mounting a plurality of semiconductor chips each having an electrode surface, comprising the steps of activating the electrode surfaces of the semiconductor chips opposite to each other; positioning the semiconductor chips opposite to each other; laminating and bonding the semiconductor chips opposite to each other by pressing without forming a reaction layer; and collectively heating the semiconductor chips so as to form the reaction layer after lamination and bonding of all the semiconductor chips are completed.

[0023]

Herein, the electrode surface includes solder formed on a bump on the semiconductor chip.

[0024]

Specifically, the reaction layer comprises a bonding layer of the solder.

[0025]

The reaction layer is uniformly formed between the semiconductor chips opposite to each other.

[0026]

Preferably, the activating step is carried out in order to remove an

organic substance on the electrode surface.

[0027]

Desirably, the pressing step is carried out in the manner such that the bonding is performed via interatomic force by making the activated electrode surfaces approach each other at an interatomic distance. Herein, supersonic wave may be applied simultaneously with the pressing step to perform lamination and bonding.

[0028]

The activating step is carried out by an atomic beam of an inactive gas excited by plasma.

[0029]

Instead, the activating step may be carried out by irradiating radical fluorine.

The activating step may be carried out by sputtering.

The activating step may be carried out by heat treatment in a reduction gas.

[0030]

The solder may be formed by electroless plating. The solder may contain an active component having a reducing action during bonding so as to use a function of substituting or helping the surface activating step.

[0031]

[Operation]

In a multi-stage laminating/mounting technique for semiconductor chips, the semiconductor chip laminating/mounting method according to this invention is characterized by providing a bonding step of carrying out lamination without heating and by heating and completing the solder bonding after completion of lamination of all layers, in contrast to the method in which heating is carried out for every stage of lamination and solder bonding is sequentially carried out and

without using temporary connection via adhesion of the flux.

[0032]

By providing the step of carrying out lamination by bonding without heating and then completing the bonding by collective reflowing, the reaction layers at the first-stage bonding portion and at the final-stage bonding portion can be formed with the same structure.

[0033]

Therefore, the thermal load is uniformly applied to the bonding portions and the semiconductor chips so as to obtain the equal bonding strength. Therefore, it is possible to avoid the situation where the reliability of the bonding portions are different depending upon high-temperature storage reliability.

[0034]

Furthermore, the semiconductor chips with the electrodes arranged at a fine pitch can be laminated with high accuracy.

[0035]

[Mode of Embodying the Invention]

Now, an embodiment of this invention will be described with reference to the drawing.

[0036]

Referring to Figs. 1(a) to (d) and Fig. 2, sectional views showing a production process according to one embodiment of this invention and a flow chart of a laminating process are shown.

[0037]

Herein, in the flow chart in Fig. 2, the semiconductor chip laminating process is generally divided into a lamination temporary bonding step 20 and a lamination heat bonding step 21.

[0038]

The lamination temporary bonding step 20 comprises a surface

activating step 201, a positioning step 202, and a pressing/superposing step 203. On the other hand, the lamination heat bonding step 21 comprises a heat bonding step 204.

[0039]

As illustrated in Fig. 1, a semiconductor chip 1 has bumps 3 formed on a circuit surface 6 and a back surface 7 thereof and solder 4 is supplied on the bumps 3. Herein, the reference numeral 2 indicates a penetration electrode.

[0040]

The semiconductor chip 1 is subjected to sputtering in a reduced-pressure atmosphere, or alternatively, irradiated with an atomic beam excited by plasma with various types of gases introduced. Thus, an organic substance on the surface of the solder 4 formed on the bump 3 is removed and the surface is activated (step 201 in Fig. 2).

[0041]

The semiconductor chip 1 to be laminated is subjected to similar treatment. Positioning is carried out in the reduced-pressure atmosphere, if necessary, in order to prevent re-contamination of the surface of the semiconductor chip 1 which has been surface-activated (step 202 in Fig. 2). Thereafter, pressing is performed (step 203 in Fig. 2).

[0042]

By pressing, the activated surface layers are made to approach each other at an interatomic distance to thereby achieve the bonding by interatomic force.

[0043]

Such bonding is carried out without heating. Therefore, a bonding reaction layer (a solder bonding layer 5) is not formed. This step enables the lamination by temporary bonding without forming the reaction layer 5.

[0044]

After a desired number of semiconductor chips are laminated in the lamination temporary bonding step 20, heating is performed to a temperature at which solder bonding is performed. Thus, lamination and mounting are completed.

[0045]

This method does not use temporary attachment by adhesive force of the flux so that a cleaning step after bonding is unnecessary.

[0046]

Further, heating and bonding are not performed during lamination but collective heating is performed after lamination of a predetermined number of semiconductor chips. This achieves an effect of forming a highly-reliable bonding portion having a uniform reaction layer for each stage of lamination. Thereafter, the laminated structure is sealed with resin, if necessary, and an external terminal is attached.

[0047]

In the aforementioned embodiment, the surface activation step and the lamination temporary bonding step for the semiconductor chips may not be carried out in the reduced-pressure atmosphere. The surface activation may be performed by irradiating an atomic beam of an inactive gas excited by plasma, irradiating radical fluorine, irradiating any other activated gas excited by plasma, irradiating any other active gas, sputtering, or heat treatment in the reduction gas.

[0048]

Further, the lamination temporary bonding step may be carried out in the reduction atmosphere under an atmospheric pressure at which the surface activity is kept, or in an inactive atmosphere.

[0049]

Moreover, the lamination temporary bonding by pressing after the

surface activation may be carried out by applying supersonic wave in addition to pressing.

[0050]

Herein, the solder 4 is supplied onto the bump 3. Alternatively, use may be made of the solder supplied by electroless plating and containing a component for activating the surface.

[0051]

The surface is activated by a reducing action of phosphorus contained in the electroless plating, thus exhibiting an effect of substituting or helping the surface activation step. The active component contained in the solder need not be phosphorus.

[0052]

Further, the solder 4 may not be supplied onto the bump 3. According to the laminating method of this invention, various combinations of copper, gold, aluminum, and other metal materials usable as the bump can be used by adjusting the method for activating the surface and the reduced-pressure environment of the atmosphere in which the lamination is performed.

[0053]

This invention is not restricted to the foregoing embodiment but may be appropriately modified within a scope of the technical concept of this invention.

[0054]

[Example]

Referring to Fig. 1, description will be made in detail about an example of this invention.

[0055]

The bumps 3 on the circuit surface 6 and the back surface 7 are formed by copper. On the bumps 3 of copper, tin is supplied to the thickness of 0.2μm-0.5μm as the solder 4.

[0056]

The semiconductor chips 1 to be laminated are prepared in an apparatus having a surface activating function and positioning, pressing, and superposing functions. After a vacuum condition on the order of $1 \times 10E^{-3}$ - $1 \times 10E^{-5}$ Pa is established, an argon gas is introduced to generate plasma and argon atoms are irradiated towards the surface of the bump for 5 minutes.

[0057]

The irradiation time depends upon the etching rate of the material supplied as the bump or the solder, and is selected within the range between 1 minute and 20 minutes. Thereafter, positioning is carried out in the reduced-pressure atmosphere and pressing is performed in order to achieve plastic deformation so that the bonding surfaces of the bumps are brought into tight contact with each other.

[0058]

Through the above-mentioned process, the temporary bonding is completed for the bumps having the activated bonding surfaces. The laminated structure temporarily bonded sequentially as mentioned above is heated to 220 °C to diffuse tin. Thus, final bonding is completed.

[0059]

Herein, the argon atomic beam in vacuum is utilized in order to activate the surface. Alternatively, use may be made of a gas excited by plasma in air. In the foregoing, pressing temporary bonding after surface activation is carried out also in vacuum. Alternatively, the bonding may be performed in air with a gas such as nitrogen or argon introduced therein.

[0060]

[Another Example]

The semiconductor chips 1 to be laminated, in which the bump 3 on the circuit surface 6 is made of gold while the bump 3 on the back surface 7 is

made of copper, are prepared in an apparatus having a surface activating function and positioning, pressing, and superposing functions. After a vacuum condition on the order of $1 \times 10E^{-3}$ - $1 \times 10E^{-5}$ Pa is established, an argon gas is introduced to generate plasma and argon atoms are irradiated towards the surface of the bump for 10 minutes.

[0061]

Positioning is carried out in the reduced-pressure atmosphere and pressing is performed in order to achieve plastic deformation so that the bonding surfaces of the bumps are brought into tight contact with each other. Thus, temporary bonding is completed.

[0062]

The laminated structure temporarily bonded sequentially as mentioned above is heated to 250 °C to execute counter diffusion of gold and copper. Thus, final bonding is completed. Herein, the heating is performed to the temperature of 250 °C. However, as far as the semiconductor chip does not cause malfunction, heating to a higher temperature is allowable. The material of the bump may be appropriately modified without any problem. A combination of metal materials is freely selected.

[0063]

[Effect of the Invention]

According to this invention, lamination is possible without forming the reaction layer at the bonding portion because temporary bonding does not require heating. By collective heating during final bonding, the uniform reaction layer is formed at the bonding portion at each stage of lamination. Thus, the structure is stabilized.

[0064]

Further, it is possible to provide a laminating method without decrease in reliability due to fusion of the electrode caused by excessive thermal

hysteresis.

[0065]

Moreover, temporary attachment by the adhesive force of the flux is not carried out so that a cleaning step after bonding is unnecessary and occurrence of migration due to the residue can be prevented.

[Brief Description of the Drawing]

[Fig. 1]

Sectional views showing a semiconductor chip laminating/mounting process according to one embodiment of this invention.

[Fig. 2]

A flow chart showing the semiconductor chip laminating/mounting process according to one embodiment of this invention.

[Fig. 3]

A sectional view showing an existing semiconductor chip laminating/mounting technique.

[Fig. 4]

Sectional views showing another existing semiconductor chip laminating/mounting technique.

[Fig. 5]

Sectional views showing another existing semiconductor chip laminating/mounting technique.

[Description of Reference Numerals]

1 semiconductor chip

2 penetration electrode

3 bump

4 solder

5 solder bonding layer

6 circuit surface

7 back surface

11 bonding wire

12 interposer

13 Ag paste

14 solder bump

15 mold resin

16 flux

[Name of Document] ABSTRACT

[Abstract]

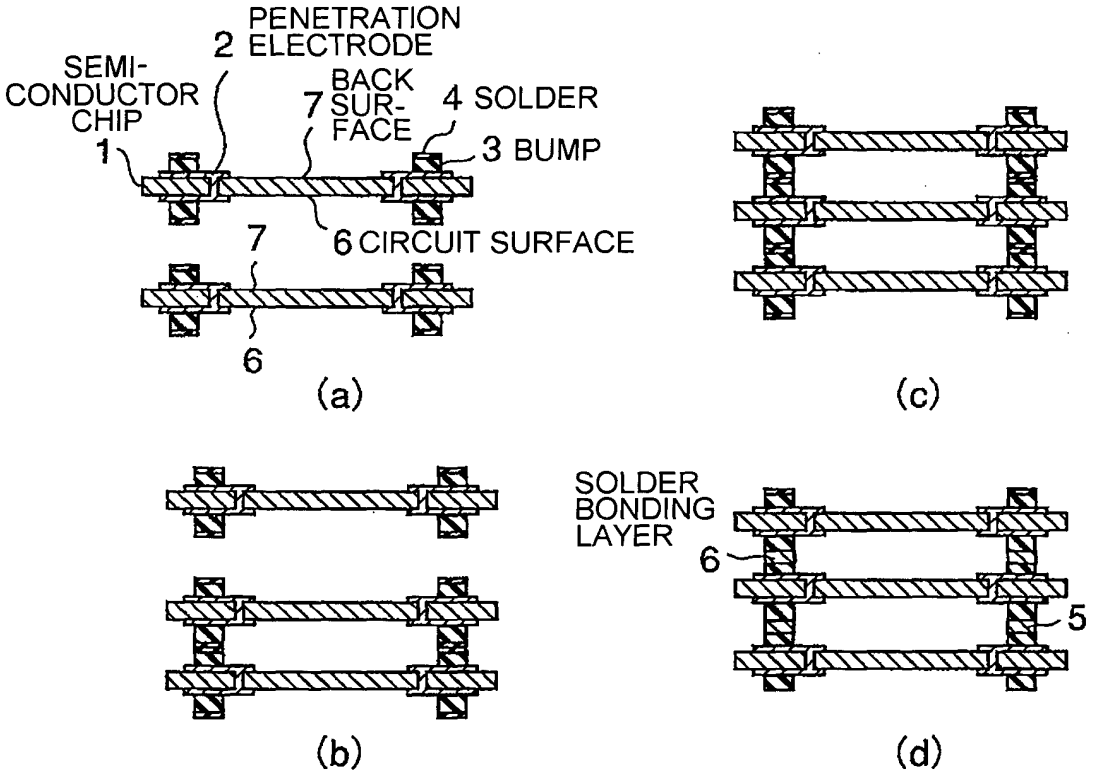
[Object] To provide a semiconductor chip laminating/mounting method capable of reducing thermal hysteresis applied to a bonding portion in lamination and mounting of semiconductor chips so that a reaction layer for each stage of lamination is uniform and improved in reliability.

[Means for Solution] A laminating/mounting method for semiconductor chips 1 is for sequentially laminating and mounting a plurality of semiconductor chips 1each having solder 4 and comprises the steps of activating the solder 4 of the semiconductor chips 1 opposite to each other; positioning the semiconductor chips 1 opposite to each other; laminating and bonding the semiconductor chips 1 opposite to each other by pressing without forming a solder bonding layer 5; and collectively heating the semiconductor chips so as to form the solder bonding layer 5 after lamination and bonding of all the semiconductor chips 1 are completed.

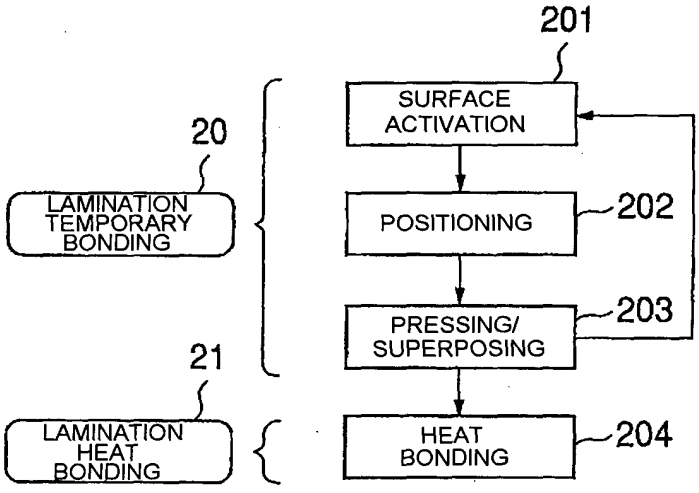
[Selected Figure] Fig. 1

[Name of Document] DRAWING

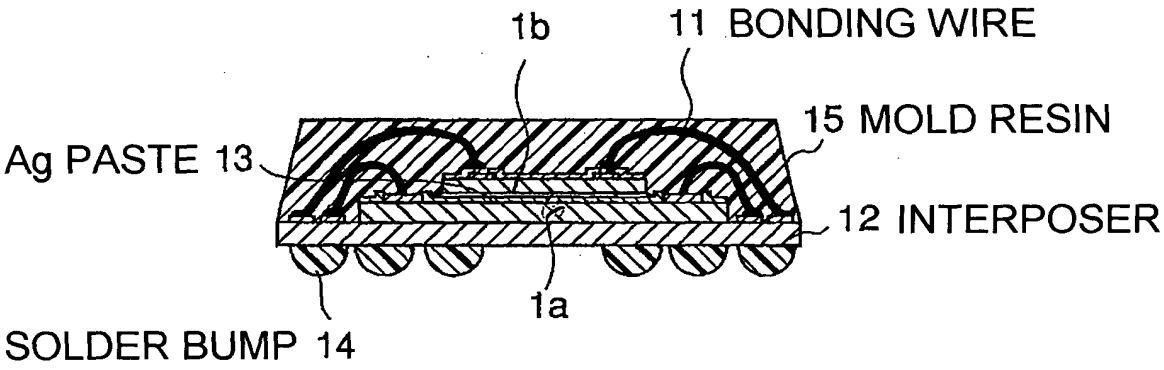
[Fig. 1]



[Fig. 2]



[Fig. 3]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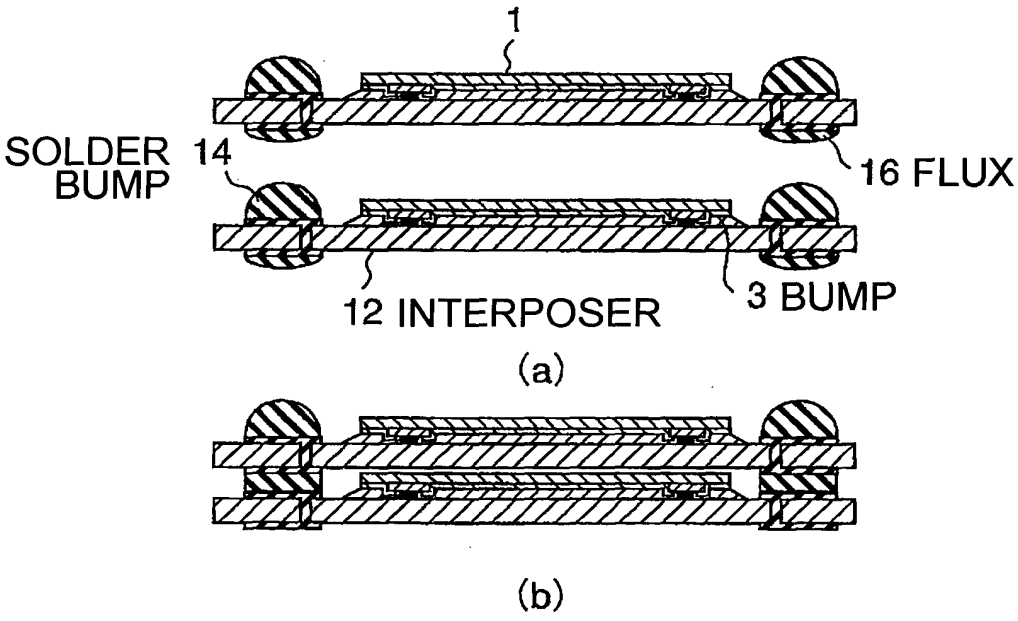
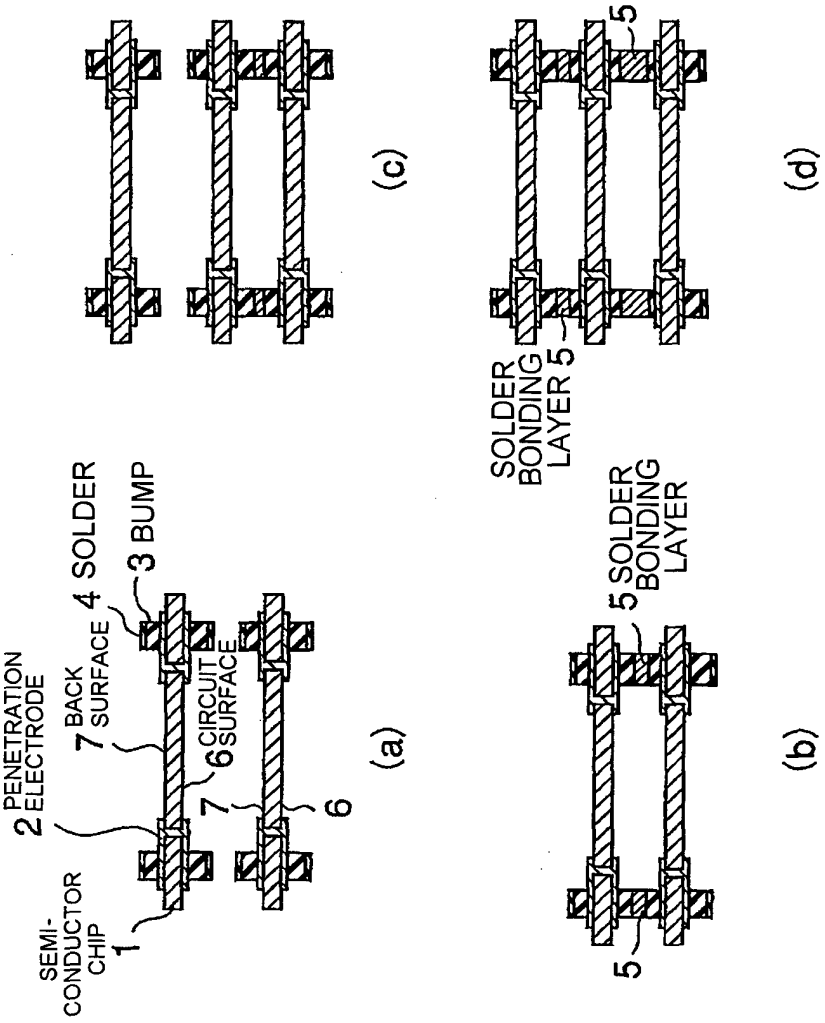
15 MOLD RESIN
Ag PASTE 13
12 INTERPOSER
1a
SOLDER BUMP 14

[Fig. 4]


1
SOLDER BUMP 14
16 FLUX
12 INTERPOSER
3 BUMP
(a)
(b)

[Fig. 5]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PENETRATION ELECTRODE 2
BACK SURFACE 7
CIRCUIT SURFACE 6
BUMP 3
SOLDER 4
(a)
SOLDER BONDING LAYER 5
(b)
(c)
SOLDER BONDING LAYER 5
(d)